Appendix C

AD2S93 Explained

The AD2S93 Converter is comprised of several sub-components, as shown in Figure C-1. In this Appendix, each of the sub-components are individually analyzed to identify a unique characteristic equation. Once each sub-component has been identified, the overall system equation for the AD2S93 is derived.

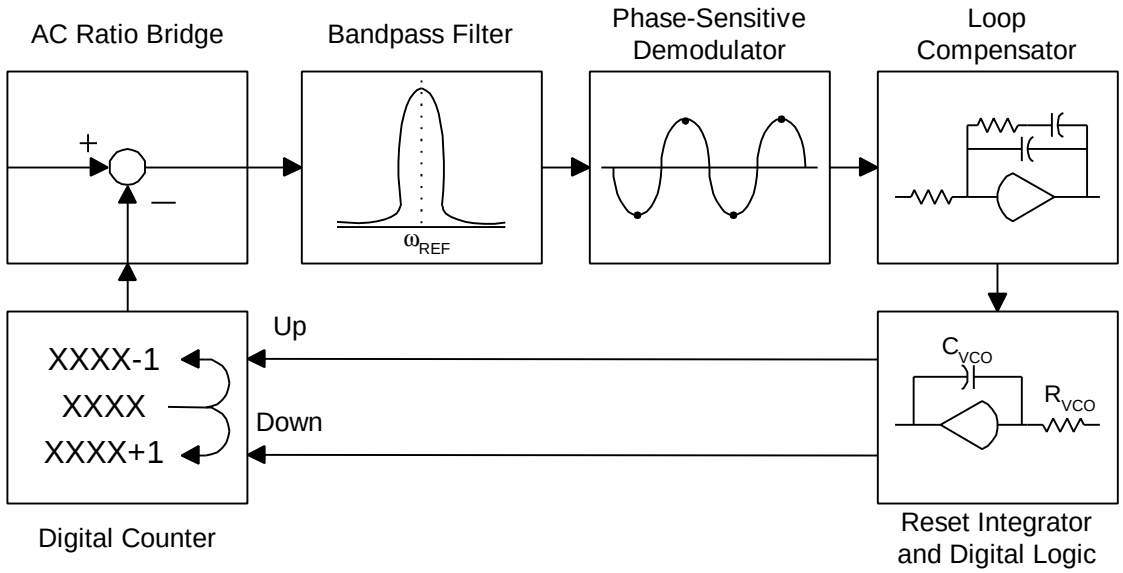

Figure C-1 - Sub-component Diagram of AD2S93

C.1 General Overview

The AD2S93 is a synchronous demodulator using a Phase Sensitive Demodulator to recover the position signal from the modulated carrier signal. The inputs to the AD2S93 are the two AC secondary winding signals from the LVDT, V_A and V_B. When the two signals are subtracted, they make up the modulated position signal, $V_{diff.}$

$$V_{diff} = (V_A - V_B)(\sin(w_c t + q)) \quad \text{(C.1)}$$

where w_c is the excitation frequency and q is the phase of the resulting signal.

The other input is V_{REF}, the reference carrier signal that is made up of the sum of the two secondary signals V_A + V_B. The output of the AD2S93 is a digital representation of the ratio of twice the V_{diff} signal over V_{REF}. As shown in Figure C-2, the center point of the LVDT is represented by the value 4096, the maximum ratio of the linear range is 8192 and the minimum value for the linear range is 0.

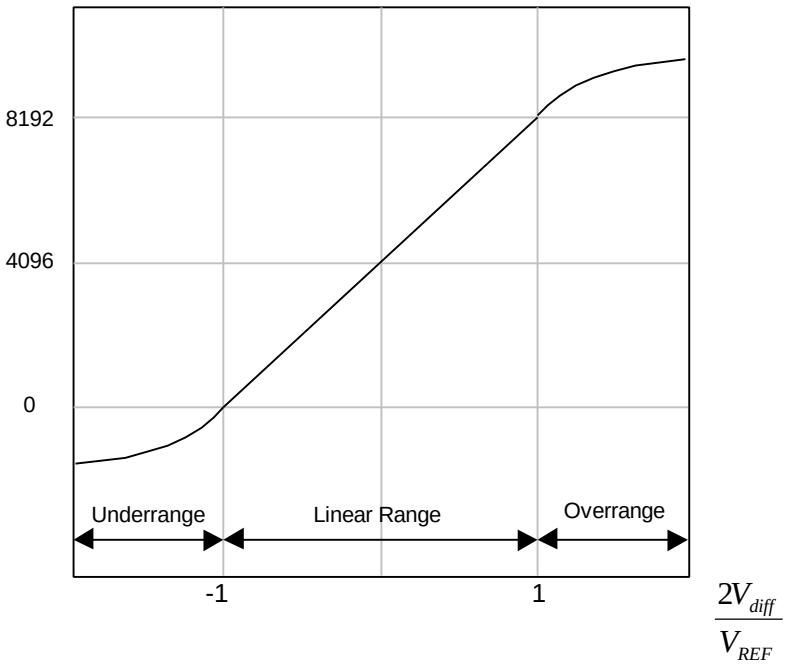

Figure C-2: Input/Output Characteristic of AD2S93

The output for any ratio beyond the linear range in Figure C-2 enters into the non-linear region of the AD2S93. These non-linear ranges are denoted as the

Overrange region (ratio greater than one) and the Underrange region (ratio less than negative one) and are neglected for the purposes of the design of the torque sensor. All motion is assumed to be within the linear range of the LVDT selected.

C.2 AC Ratio Bridge

The AC Ratio Bridge is the subsystem that provides the input interface to the AD2S93 and provides the subtraction function necessary to generate the error signal that is required for the tracking loop. An approximate functional representation of the AC Ratio Bridge subsystem is shown in Figure C-3.

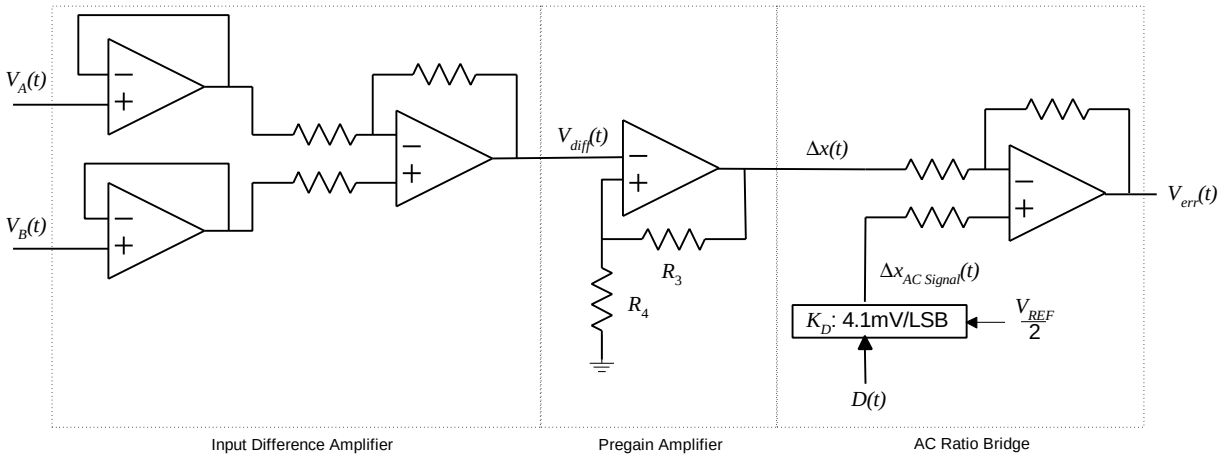

Figure C-3: Estimated Structure for AC Ratio Bridge

The Input Difference Amplifier creates the AC difference signal V_{diff} from the two input signals, V_A and V_B. The Pregain Amplifier, set by external resistors, amplifies the difference signal to provide increased sensitivity to the motion of the core. The resulting signal, $\Delta x(t)$, is then passed to the AC Ratio Bridge.

Figure C-3 also shows a functional analog to the operation of the AC Ratio Bridge as a simple subtractor circuit. Closer inspection shows that the AC Ratio Bridge more closely resembles a multiplying digital-to-analog converter (DAC), where the digital word is used to determine which input signal to the DAC is applied to each stage of the resistive bridge network. By applying the amplified

V_{diff} signal or the V_{REF} signal to the resistive bridge network, the AC Ratio Bridge provided in a very fast subtraction operation.

The system equation for describing the AC Ratio Bridge is expressed in Equation (C.2).

$$V_{Err} = K_{pregain}\left(V_A - V_B\right) - K_{Dword}\frac{V_{REF}}{2} \qquad \text{(C.2)}$$

where

$$K_{pregain} = 1 + \frac{R_3}{R_4} \qquad \text{(C.3)}$$

$$K_{Dword} = 1 - \frac{D}{4096}, \qquad D \in [0,8192] \qquad \text{(C.4)}$$

where R_3 and R_4 are the gain resistors for the pregain amplifier.

C.3 Bandpass Filter

The AD2S93's passive second-order bandpass filter, as shown in Figure C-4, is constructed with two capacitors and two resistors. The value of the components are determined by the desired center frequency, f_{REF}, and Equations (C.5) and (C.6).

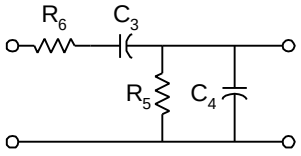

Figure C-4 : Bandpass Filter

$$15k\Omega \le R_5 = R_6 \le 56k\Omega \qquad \text{(C.5)}$$

$$C_3 = C_4 = \frac{1}{2pR_5 f_{REF}} \qquad \text{(C.6)}$$

Once the components have been selected, the center frequency of the bandpass filter is defined in Equation (C.7).

$$f_{REF} = \frac{1}{2pR_5C_4} = \frac{1}{2pR_6C_3} \qquad \text{(C.7)}$$

The transfer function of the bandpass filter between the input and output voltage, $V_{in}(s)$ and $V_{out}(s)$ can be obtained.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_6 C_3 s}{R_5 R_6 C_3 C_4 s^2 + (R_5 C_3 + R_6 C_4 + R_6 C_3)s + 1} \quad \text{(C.8)}$$

When $R_5 = R_6 = R$ and $C_3 = C_4 = C$, the transfer function reduces to a simpler form.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{RCs}{R^2 C^2 s^2 + 3RCs + 1} = \frac{1}{3 + \left(RCs + \frac{1}{RCs}\right)} \quad \text{(C.9)}$$

Substituting $s = jw$ and $w_0 = \frac{1}{RC}$ into Equation (C.9), the transfer function becomes:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{3 + j\left(\frac{w}{w_0} - \frac{w_0}{w}\right)} \quad \text{(C.10)}$$

Equation (C.10) shows that, at the center frequency, the imaginary term of the bandpass filter vanishes and the filter has a maximum gain of 1/3 with zero phase shift. In the AD2S93, the center frequency is tuned to the carrier frequency to attenuate out extraneous noise from the modulated signal. If the position information carried by the modulated signal is a simple DC term, then this component is a simple gain stage with no phase contribution. However, when analyzing this block within the bandwidth of the position signal (i.e. 0 - 100Hz), the filter adds up to four degrees (4°) of phase shift to the position signal. As a separate unit, the amount of phase shift contributed by the bandpass filter should not cause any loss of tracking of the AD2S93. For completeness, the phase contribution is modeled for control design purposes.

Linearizing the transfer function about the center frequency provides an approximation of the dynamic contribution of the bandpass filter to the overall system. If $w = w_0 + \partial w$, the bandpass filter transfer function can be rewritten as follows:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{3 + j\left(\frac{2\partial w}{w_0} - \frac{\partial w^2}{w_0(w_0 + \partial w)}\right)} \approx \frac{1}{3 + j\left(\frac{2\partial w}{w_0}\right)} \qquad \text{(C.11)}$$

By substituting $s = j\partial w$, the approximation for the demodulated bandpass filter takes on the characteristics of a single pole, low-pass filter with a corner frequency of $\frac{3w_0}{2}$.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{w_0}{2}\frac{1}{s + \frac{3w_0}{2}} \qquad \text{(C.12)}$$

C.4 Phase Sensitive Demodulator

The Phase Sensitive Demodulator (PSD) is the most significant subsystem of the AD2S93 Converter since it provides the demodulation of the position signal which is used by the remainder of the tracking loop.

The reference signal V_{REF} is fed into the PSD and phase shifted by -90° through a second order low pass filter. By performing this phase shift, the zero crossings of V_{REF} are aligned with the peaks of the modulated position signal. As the phase-shifted V_{REF} signal hits a zero crossing, the modulated position signal's peak is sampled and held until the next zero crossing. The sign of the slope from the reference signal and the sign of the position signal's peak determines the sign of the sample. The resulting sample-and-hold signal is the demodulated position signal. This process is shown in Figure C-5.

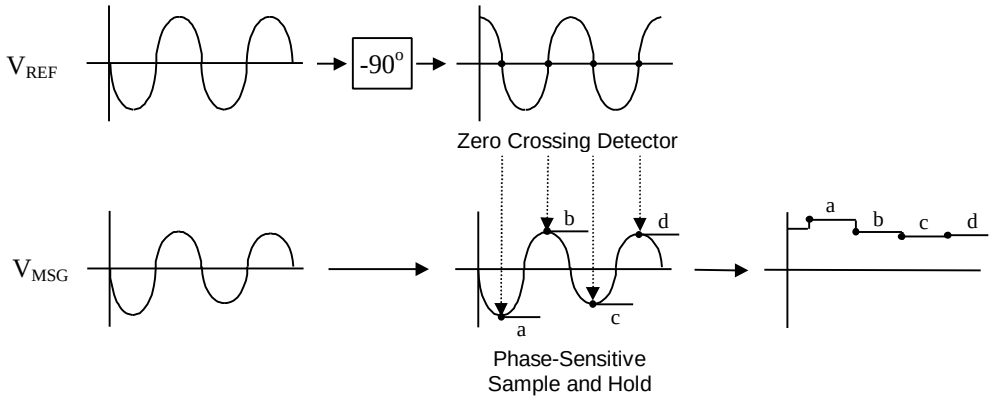

Figure C-5: Functional Depiction of Phase Sensitive Demodulator

The PSD can be seen, in the demodulated domain, as a simple unity amplifier, since the demodulation of the position incurs no attenuation. Therefore, the subsystem equation would be a gain of 1.0.

C.4.1 Problems with the Phase Sensitive Demodulator

In actual operation the PSD works as described, but, with additional, undesirable characteristics. In the case of a constant position signal with constant amplitude, the output of the PSD resulted in a small squarewave signal. In this case, V_{MSG} can be defines as a constant sinewave.

$$V_{MSG} = A\sin(w_c t) \tag{C.13}$$

As shown in Figure C-6, the constant amplitude signal V_{MSG} does not result in a constant demodulated position signal.

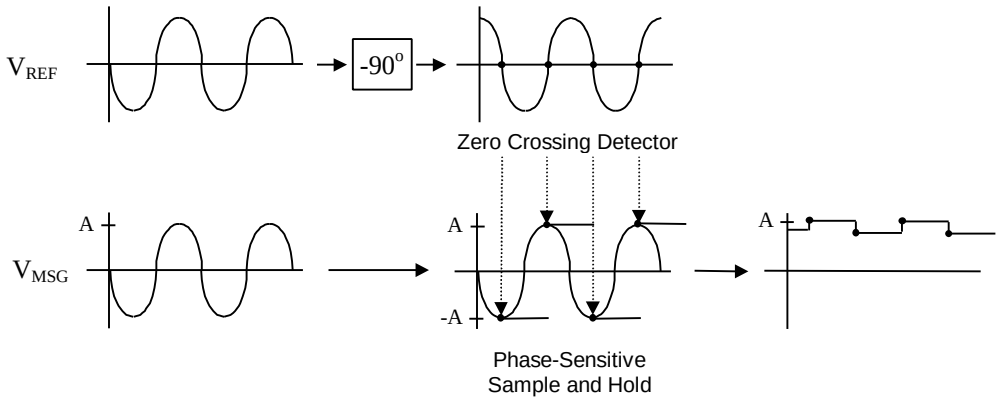

Figure C-6: Problem with Tracking Constant Position

The cause for this action is unknown, but a hypothesis is offered to explain this action. The actual sample and hold circuit used in the AD2S93 is a pair of capacitors that are switched in and out of a voltage follower circuit as the zero crossing detector senses the reference signal cross the zero value. As shown in Figure C-7, at an even zero crossing, the first capacitor provides the voltage signal to the voltage follower while the second capacitor charges up with the incoming modulated signal. Given that R_{in} results in a fast time constant, the capacitor charges up to the maximum value before the next zero crossing. At the

next zero crossing, the capacitors switch and the second capacitor becomes the source voltage, with its voltage read from the reverse direction, providing the necessary sign change for tracking the second half of the signal. The first capacitor then charges until the next zero crossing and the cycle repeats.

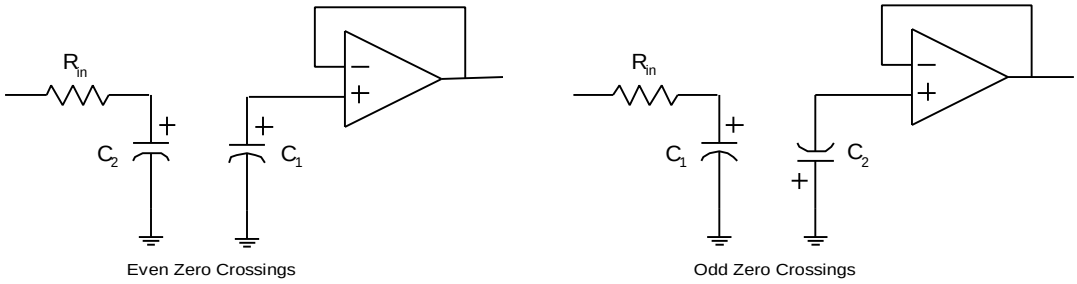

Figure C-7: Description of Switching Capacitors in PSD

Since the zero crossing circuit is driven by the squared off phase-shifted reference signal, any DC biases that exist in the reference signal can cause the points which are sampled to have a different sampling period between them. The result is a peak detector that incorrectly captures the position signal half of the time and thus results in the square wave as shown in Figure C-8.

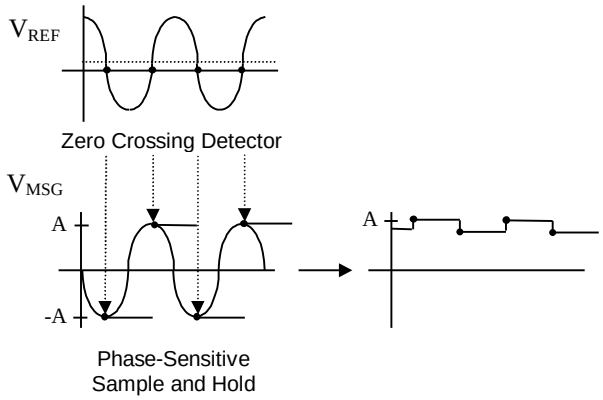

Figure C-8: Demonstration of Faulty Zero Crossing Detector

A telltale sign of this effect is found when analyzing the duty cycle between the different transitions determining how much time elapses between the positive transition and the negative transition. In experimentation, testing with a pure AC signal (zero DC bias) for the reference signal provided a slightly smaller square wave with a duty cycle close to 50%. Variances or delays existing in the

switching values in the zero crossing circuit could explain the remaining square wave signal.

With this problem, the system equation for the PSD, as a simple gain circuit is problematic. For the gain of the system, it is assumed that if the PSD works perfectly, a gain of one would be enough. This premise assumes that the -90 degree phase shift occurs to capture the peaks of the modulated position signal. The low pass filter used in the AD2S93 provides a -93.5 degree phase shift for the reference signal. Hence, the gain is approximately 1.0, but, not exactly, 1.0. With the addition of the square wave on the output of the PSD at twice the frequency of the reference signal, the PSD becomes an additive noise source. However, for the purposes of design, the system equation for the PSD is assumed to be a simple gain circuit with a gain of 1.0.

C.5 Voltage Controlled Oscillator and Digital Counter

The Voltage-Controlled Oscillator (VCO) and the Digital Counter make up the digital interface of the AD2S93 and are considered the "plant" of the control system that the Loop Compensator controls. The VCO is a reset integrator with a discharge circuit that releases the capacitor's charge when the voltage seen on the output of the VCO is plus or minus 250 millivolts. The gain on the VCO is set by an internal resistor that is either connected in parallel (VCO GAIN to VEL) or left disconnected, as shown in Figure C-9.

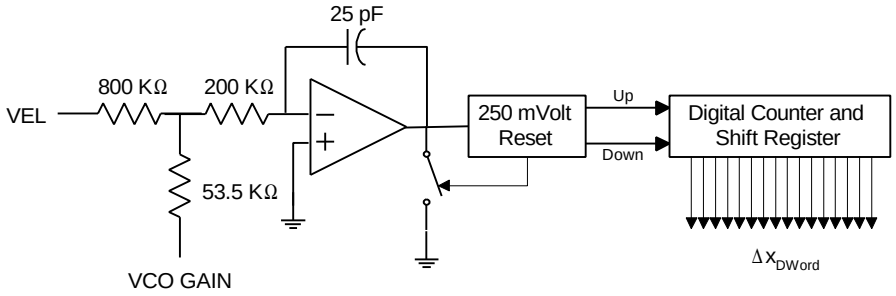

Figure C-9: AD2S93 VCO and Digital Counter

As the signal from the Loop Compensator is applied to the VCO, the capacitor is charged and the output integrates to either 250 or -250 millivolts. When the reset voltage is reached, the counter is either incremented or decremented in accordance with the sign of the VCO output and the VCO capacitor is immediately discharged.

The 16-bit Digital Counter has thirteen bits assigned to the LVDT position and three bits assigned to status flags for the AD2S93. The first three bits represent Loss of Signal (LOS), Overrange (OVR) and Underrange (UNR) as discussed in Section C.1. The remaining thirteen bits represent the linear region of the AD2S93 and can be mapped to the region shown in Figure C-2.

The system equation for the combination of the VCO and the shift register is represented as a simple integrator with an adjustable gain.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{K_{INT}}{s} \tag{C.14}$$

where the integrator gain K_{INT} is defined:

$$K_{INT} = \frac{1}{(25pF)(1M\Omega)(250mV)} = 160K \text{ for Mode 1} \tag{C.15}$$

$$K_{INT} = \frac{1}{(25pF)(250K\Omega)(250mV)} = 640K \text{ for Mode 2} \tag{C.16}$$

C.6 Loop Compensator

Completing the AD2S93 tracking loop is the Loop Compensator which provides the control law necessary for tracking the modulated position signal. The Loop Compensator is made up of a single operational amplifier, which receives the output of the PSD, processes the signal, and then passes the result to the output to the VCO. Due to the design of the AD2S93, only the ends of the internal $25k\Omega$ resistor and the output of the amplifier are available for external modification. Additionally, the AD2S93 electronics circuit board allows component configuration as shown in Figure C-10 where R_7, R_8, R_2, C_1 and C_2 may be modified by the designer.

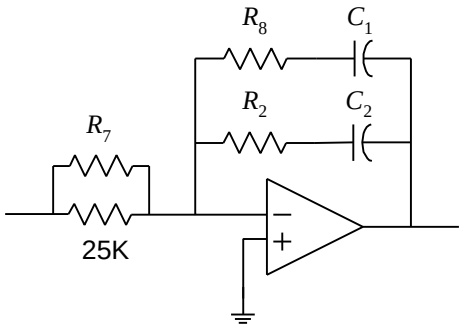

Figure C-10: Loop Compensator with Potential Components

The limited number of possible modifications admit only a small number of controller designs. From this subset, two specific controllers are selected for testing, one provided by Analog Devices and one devised in the ARTISAN lab.

C.6.1 Analog Devices Solution

The initial architecture for the AD2S93 evolved from another component in the Analog Devices family, the AD2S80, a Resolver-to-Digital Converter. Since a resolver operates on the principle of continual rotary motion to determine its position, the tracking loop for the AD2S80 requires zero error in velocity as well as position. With this requirement, the Loop Compensator needs to include a second integrator to provide the characteristics of a Type II system. To compensate the system, Analog Devices includes a lead network to provide additional phase and bandwidth on the closed loop system. Figure C-11 shows the structure of the suggested compensator provided by Analog Devices and Equation (C.17) provides the system equation of this system.

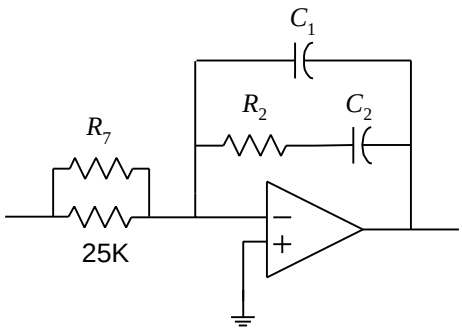

Figure C-11: Analog Devices Suggested Loop Compensator

$$\frac{V_{out}(s)}{V_{in}(s)} = K_{LC}\frac{s+z}{s^2+ps} \tag{C.17}$$

where

$$K_{LC} = \frac{1}{(R_7 \| 25K\Omega)C_1} \tag{C.18}$$

$$z = \frac{1}{R_2 C_2} \tag{C.19}$$

$$p = \frac{C_1 + C_2}{R_2 C_1 C_2} \tag{C.20}$$

When the above compensator is implemented using the component selection algorithm discussed in Appendix B, the best performance achieved provides a bandwidth of no more than 600 Hz with an overshoot of 34%, as shown in Figure C-12.

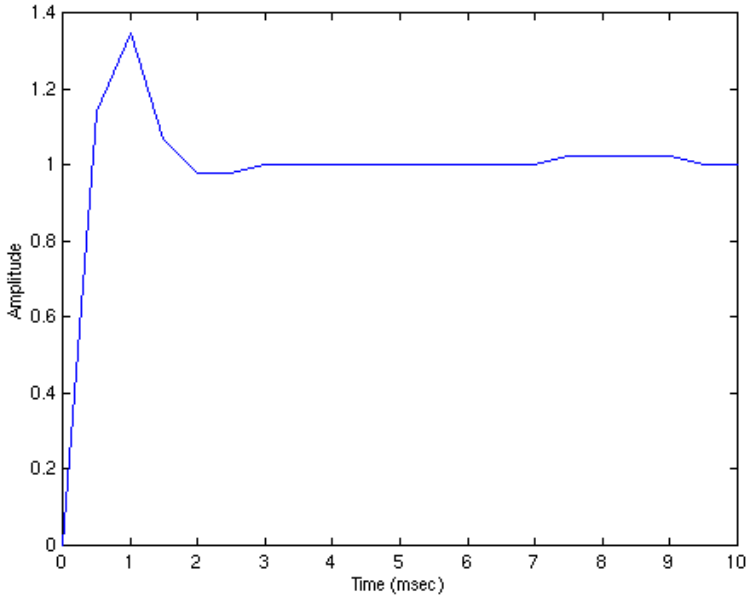

Figure C-12: Step Response of AD2S93 Compensator

The overshoot is a damaging characteristic in the torque sensor because it provides a phantom torque that the torque control loop attempts to compensate. The overshoot is not easily adjusted because of the lead compensator zero that limits the bandwidth and provides derivative action that excites the overshoot.

Therefore, a compensator that does not include derivative control would provide the necessary response.

C.6.2 ARTISAN Solution

Since the design of the Analog Devices compensator is based on the need for a Type II System, the first step in redesigning the compensator is to eliminate this need. Additionally, LVDTs do not require constant velocity tracking, only zero steady-state position error. Since the VCO/Digital Counter provides the integrator necessary for the Type I loop, the Loop Compensator has a number of possibilities within the constraints of the AD2S93 component selection. Possible ompensators include:

- Gain – where the system is a simple gain
- Lead – providing additional phase and attenuation at the higher frequencies
- Low Pass Filter – providing gain and attenuation in selected frequency ranges

Testing these potential solutions, a number of results were developed. The gain compensator solution was unable to stabilize the output of the AD2S93 for any value of the gain. The lead compensator provided stability and fast response, but a very long settling time and thus a very slow steady state error response. The Low Pass Filter provided the best performance, allowing for an increase in the gain in the low frequencies and an attenuation of the high frequency square wave noise generated by the PSD. The ARTISAN Loop Compensator has the structure shown in Figure C-13 and the system equation in Equation (C.21). It had a bandwidth of 800 Hz with very little overshoot as shown in Figure C-14.

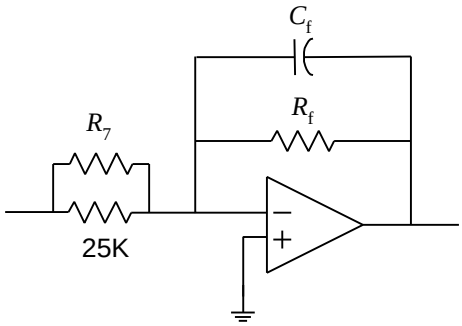

Figure C-13: ARTISAN Low Pass Filter Compensator

$$\frac{V_{out}(s)}{V_{in}(s)} = K_{LC}\frac{1}{s+p} \tag{C.21}$$

where

$$K_{LC} = \frac{1}{(R_7 \| 25K\Omega)C_f} \tag{C.22}$$

$$p = \frac{1}{R_f C_f} \tag{C.23}$$

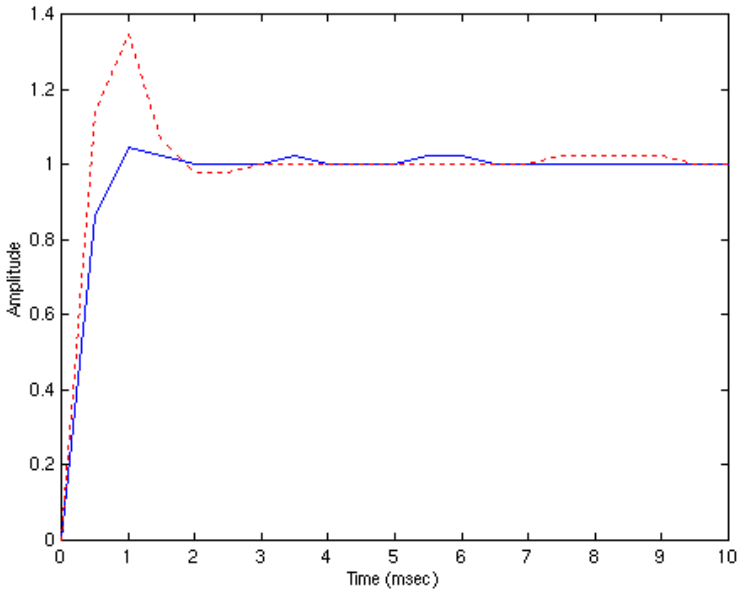

Figure C-13: Step Responses of Analog Devices Compensator (dashed) and ARTISAN Compensator (solid)

C.7 Combining the System Equations

Once all of the system equations have been determined, closing the loop on the system, given the ARTISAN Low Pass Filter compensator, results in the following system equation with the performance shown in Figure C-13.

$$\frac{\Delta x_d}{\Delta x_v} = \frac{K_{AC}K_{BP}K_{PSD}K_{INT}}{\left(s + w_{BP}\right)\left(s^2 + ps\right) + K_{AC}K_{BP}K_{PSD}K_{INT}} \tag{C.24}$$

where

$$K_{AC} = 4.1e-3 \tag{C.25}$$

$$K_{BP} = \frac{w_0}{2} \tag{C.26}$$

$$w_{BP} = \frac{3w_0}{2} \tag{C.27}$$

$$K_{PSD} = 1 \tag{C.28}$$